VANSHIKA GHAI

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About Me

PhD Scholar at IIT Bhubaneswar, working in Semiconductor Device Modeling and Simulation with a focus on circuit-device co-optimization using TCAD. Interested in reliability-aware device design, self-heating effects, stress engineering, and advanced CMOS technologies.

EDUCATION

Course	Institution	Year	CPI
Doctor of Philosophy (Pursuing)	Indian Institute of Technology Bhubaneswar, Odisha	2025 -	——
Master of Technology in VLSI Design & Embedded systems	National Institute of Technology, Raipur, Chhattisgarh	2023 - 2025	9.08
Bachelor of Technology in Electronics & Teleommunication	Bhilai Institute of Technology, Durg, Chhattisgarh	2019 - 2023	9.0

TECHNICAL SKILLS

Software & Hardware Languages : Verilog, System Verilog, UVM, VHDL, Java, JavaScript, C, C++
Design and Simulation Tools : Sentautus TCAD, Cadence Virtuoso, Xilinx Vivado, Silvaco TCAD, Xilinx ISE Design Suite, Xilinx Vivado, MATLAB, LTspice, HSPICE, PSpice.

Key Projects

1. Cyclic Redundancy Check

   Cyclic Redundancy Check is an error detection method commonly used in digital networks and storage devices. Designed it using Verilog HDL and successfully conducted the verification process using Xilinx ISE Design Suite software.

2. Two Stage OPAMP

   Designed and simulated a two-stage operational amplifier using LTspice simulator software to optimize performance metrics such as CMRR, gain, bandwidth, power consumption.

3. Dual Port Ram

   Implemented a dual-port RAM using Xilinx ISE Design Suite using Verilog HDL to model and successfully conducted the verification process using System Verilog HDL.

Key Projects

4. Phase-Locked Loop

   Designed and simulated a Phase-Locked Loop (PLL) using Cadence Virtuoso to achieve precise frequency generation and synchronization. Also made layout design of same in Virtuoso.

Publications

1. Ghai, Vanshika & Dash, Sidhartha & Mishra, Guru. (2025). Reliability assessment of graphene channel vertical TFET: Role of trap-assisted tunneling. Microelectronics Reliability. 175. 115943. 10.1016/j.microrel.2025.115943.
2. Singh, Ragini & Ghai, Vanshika & Naugarhiya, Dr. Alok & Mishra, Guru. (2025). A Virtually Doped Hetero Z-Shaped Charge Plasma TFET Based Label Free Biosensor. Sensing and Imaging. 26. 10.1007/s11220-025-00621-6.
3. Vaishnaw, Anita & Jaiswal, Aashutosh & Gajananrao, Bhange & Ghai, Vanshika & Mishra, Guru. (2025). Enhancement of switching current ratio with workfunction modulated SiGe Vertical TFET. 429-432. 10.1109/DevIC63749.2025.11012214.
4. Sharma, Meenu & Ghai, Vanshika & Dash, Sidhartha & Mishra, Guru. (2024). Double Gate Tunnel FET with Core-Gate Engineering: An Effective Approach to Suppress Ambipolarity. 314-317. 10.1109/EDKCON62339.2024.10870762.

LEADERSHIP SKILLS

- Trainer

  High End Workshop (KARYASHALA) on "Exploring Semiconductor Devices: A Practical Approach to VLSI" The workshop was organized by the Department of ECE, National Institute of Technology, Raipur, in association with SERB, Government of India.

- Teaching Assistant (August 2024 - Present)
  - Conducted Verilog Labs for MTech 26' batch at NIT Raipur
  - Conducted Cadence Labs for MTech 26' batch at NIT Raipur
  - Conducted Introduction to Electronics Lab for BTech (CSE) 29' batch at IIT Bhubaneswar
  - Conducted VLSI Design Lab & Tutorial for BTech (CSE) 29' batch at IIT Bhubaneswar